Two's Complement

Electrical Engineering

The signed representation that lets one adder serve both signed and unsigned work.

Two's complement lets one adder circuit handle both signed and unsigned arithmetic.

Negate: invert every bit, then add 1

−5 in 8 bits — **1111 1011**

Invert 5, add 1.

8-bit range — **−128 to +127**

One extra negative.

Top bit is 1 — **The value is negative**

Sign bit.

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× **Reading the carry out as signed overflow**

✓ **Overflow is a disagreement of signs**

Signed overflow happens when both operands share a sign and the result does not. Carry out is the unsigned indicator, a different flag.

There is no negative zero, which is why the range is asymmetric. Sign extension copies the top bit into every new position.