State Machine Design

Electrical Engineering

From a written specification to a single-clock synchronous machine, in six moves.

Get the states right first; the logic afterwards is mechanical.

1. **List the states**
   One state per situation the machine must actually remember, and no more.

2. **Draw the state diagram**
   Label every arc with its condition, and cover every input combination.

3. **Choose Moore or Mealy**
   Moore outputs depend on state alone; Mealy also on the present input.

4. **Encode and tabulate**
   Binary, Gray or one-hot, then tabulate next state and output per state.

5. **Derive the logic**
   One flip-flop per state bit, driven by combinational next-state logic.

6. **Handle unused states**
   Give every unreachable code a defined exit back to a known state.

Moore machines are glitch-free but answer a cycle later. Mealy machines answer at once and pass input glitches to the output.