Setup & Hold Time

Electrical Engineering

The two timing windows around a clock edge, and the very different fixes each needs.

Data must be stable for the setup time before a clock edge and for the hold time after it.

$$T_{clk} \geq t_{cq} + t_{logic} + t_{setup} + t_{skew}$$

0.4 + 3.2 + 0.3 ns — **3.9 ns per cycle**

Ignoring skew.

Maximum clock — **About 256 MHz**

1 ÷ 3.9 ns.

Hold violation — **Add path delay**

Not a slower clock.

THE COMMON MISTAKE

× Slowing the clock to fix a hold violation

✓ Adding delay to the offending short path

Hold time depends on the fastest path after an edge, not on the clock period, so a slower clock changes nothing at all.

Violating either window risks metastability. Synchronising an asynchronous input takes two flip-flops in series, never one.