Latches vs Flip-Flops

Electrical Engineering

Level-sensitive against edge-triggered storage, and why synchronous design picks one.

Latch, level sensitive

- Transparent while the enable is high
- Output follows the input during that window
- Fewer transistors, less silicon area
- Hard to time and hard to test
- Glitches pass straight through it

Flip-flop, edge triggered

- Samples only on a clock edge
- Output holds for the whole cycle
- One clean sampling instant per cycle
- Setup and hold windows are well defined
- The basis of synchronous design

THE DIFFERENCE THAT MATTERS

Synchronous design uses flip-flops so that every logic path gets exactly one clock period to settle.

An inferred latch in HDL nearly always means an incomplete if or case statement, and it is a warning worth chasing down.